Summary Report

The prelab before lab 1 prepared the lab with an introduction to the class server, terminal, and the cad tools. Once connected the VLSI server you can then begin lab 1 where it starts out setting up the shell environment which is TCSH. This is where lab 1 begins: create a folder for the class and extract the lab 1 materials from the website using atool. Once in the terminal with the materials you can begin initializing the design compiler, where we are using Nangate45 PDK (process design kit).

To synthesis our first circuit we had to obtain a vhdl file (with code) (adder 64), where are able to prepare a script and perform the synthesis. Looking for the dc.tcl (tcl script) to control the design compiler we are then given definitions to basic tcl syntax. Running the compiler required a dc\_shell -f dc.tcl (dc.tcl is the tcl scripts) and | tee dc.log is copying back to a log.

After running the 64-Bit adder, another circuit was synthesized in FPGen. Reports are given in dc.rpt

The main objective for lab 1 was to create a 128-adder circuit which consisted of changing a few variables in the 64-bit adder. Since only 64 bits were in the adder changing it from input [63:0] and output [63:0] sum; … I switched it out with 127. Once done running the synthesis script on the 128-adder using the dc.tcl script from the same 64-bit adder generated a report (using the same script is okay, because it’s just obtaining information to generate the circuit not the actual inputs of the circuit). After running the synthesis, the reports from the previous circuits are to be compared with the circuit made (128-bit adder) and that is the end of lab 1.

Comparison:

Date Arrival Time Total Cell Area Total Power

Adder64: 5.85 272.384003 282.1547 uW

FPGen: -1.66 13023.892119 1.4488e+04 uW

Adder128: 11.65 544.788005 568.0502 uW

FPGEN has the lowest Arrival Time | ADDER64 has the lowest cell area | ADDER64 has the lowest power

ADDER128 has the high Arrival Time | FPGEN has the largest cell area | FPGEN has the high power